In the Claims:

Claim 1 (previously presented): A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

an epitaxially formed semiconductor layer of a second conductivity type formed over said substrate;

a body region of said first conductivity type formed in said epitaxially formed semiconductor layer, said epitaxially formed semiconductor layer extending below said body region;

a source region of said second conductivity type formed in said body region, said source region being adjacent an invertible channel in said body region;

a gate structure formed over said invertible channel region, said gate structure including a gate electrode which is spaced from said invertible channel by a gate insulation layer;

a drain region of said second conductivity type formed in said epitaxially formed semiconductor layer, said drain region and said body region being spaced from one another by a drift region in said epitaxially formed semiconductor layer;

a resurf region of said first conductivity type formed in said epitaxially formed semiconductor layer, said resurf region being formed over at least a portion of said drift region in said epitaxially formed semiconductor layer between said body region and said drain region and adjacent to and in contact with said drain region; and

a field plate structure disposed over said resurf region, said field plate structure including a first field plate disposed over a first insulation layer of a first thickness extending from said gate insulation layer, a second field plate disposed over a second insulation layer of a second thickness, said second insulation layer being formed over said first insulation layer, and a third field plate spaced from said second field plate by a third insulation layer of a third thickness, wherein said first field plate includes a first portion spaced from a second portion by a first gap, said first portion of said first field plate extending from said gate electrode, said second portion of said first field plate electrically connected to said drain region, said second field plate includes a first portion spaced from a second portion by a second gap, and said third field plate includes a first portion spaced from a second portion by a third gap, and wherein said first gap is wider than said second gap and said third gap, and said second gap is wider than said third gap, and wherein said gaps are filled only with an insulation material; and

wherein said first portion and said second portion of said second field plate, and said first portion and said second portion of said third field plate are disposed around said drain region, wherein said semiconductor device exhibits a breakdown voltage of at least 600 volts.

Claim 2 (original): A semiconductor device according to claim 1, wherein said first insulation layer is comprised of an oxide.

Claim 3 (original): A semiconductor device according to claim 1, wherein said first thickness is 0.4 microns.

Claim 4 (original): A semiconductor device according to claim 1, wherein said second insulation layer is comprised of an oxide.

Claim 5 (original): A semiconductor device according to claim 1, wherein said second thickness is 1.3 microns.

Claim 6 (original): A semiconductor device according to claim 1, wherein said third insulation layer is comprised of an oxide.

Claim 7 (original): A semiconductor device according to claim 1, wherein said third thickness is 1.4 microns.

Claim 8 (canceled)

Claim 9 (previously presented): A semiconductor device according to claim 1, wherein said first field plate is comprised of conductive polysilicon.

Claim 10 (canceled)

Claim 11 (previously presented): A semiconductor device according to claim 1, wherein said second gap is 45 microns.

Claim 12 (canceled)

Claim 13 (previously presented): A semiconductor device according to claim 1, wherein said third gap is 25 microns.

Claims 14-19 (canceled)

Claim 20 (previously presented): A semiconductor device according to claim 1, wherein said first portion of said first field plate terminates below said first portion of said second field plate.

Claim 21 (previously presented): A semiconductor device according to claim 1, wherein said second portion of said second field plate is electrically connected to said drain region, and to said second portion of said third field plate.

Claim 22 (previously presented): A semiconductor device according to claim 1, wherein said first portion of said second field plate is electrically connected to said first portion of said first field plate.

Claim 23 (previously presented): A semiconductor device according to claim 1, wherein said first portion of said third field plate is electrically connected to said source region.

Claims 24-29 (canceled)

Claim 30 (currently amended): A field plate structure for a laterally diffused high voltage semiconductor device, said field plate structure comprising:

a first field plate having a first portion and a second portion separated by a first gap, wherein said first field plate is disposed over a first insulation layer on top of a reduced surface field drift region of said laterally diffused high voltage device;

a second field plate having a first portion and a second portion, said first portion of said second field plate electrically connected to said first portion of said first field plate, said first portion and said second portion separated by a second gap, wherein said second field plate is disposed over said first field plate by a second insulation layer, and wherein said second gap is narrower than said first gap.

Claim 31 (previously presented): The field plate structure of claim 30, wherein said first portion of said first field plate is electrically connected to a gate electrode of said laterally diffused high voltage semiconductor device.

Claim 32 (previously presented): The field plate structure of claim 30, wherein said second portion of said second field plate is electrically connected to a drain region of said laterally diffused high voltage semiconductor device.

Claim 33 (previously presented): The field plate structure of claim 30, wherein said second portion of said first field plate is electrically connected to said second portion of said second field plate.

Claim 34 (previously presented): The field plate structure of claim 30, further comprising a third field plate having a first portion and a second portion separated by a third gap, wherein said third field plate is disposed over said second field plate by a third insulation layer, and wherein said third gap is narrower than said second gap.

Claim 35 (previously presented): The field plate structure of claim 34, wherein said first part of said third field plate is electrically connected to a source of said laterally diffused high voltage semiconductor device.